Claims

[c1] What is claimed is:

1.An encoding method for an optical recorder, the optical recorder comprising an encoder for encoding data received from a computer, and a processor for controlling operations of the encoder, the encoding method comprising:
receiving data of a next mode which is different from a current mode from the computer even when the encoder is still encoding data of the current mode.

[c2] 2.The encoding method of claim 1 wherein the optical recorder further comprises a buffer for storing data transmitted from the computer, the encoding method further comprising:
storing data received by the encoder from the computer into the buffer.

[c3] 3.The encoding method of claim 1 wherein the data is transmitted to the encoder through an IDE bus.

[c4] 4.The encoding method of claim 2 wherein the encoder comprises:
a host interface for receiving data from the computer;
an encoder sector processor for encoding data according to modes of the data;
an encoder buffer arbiter connected to the host interface, the buffer and the encoder sector processor for storing data from the host interface into the buffer, transferring data in the buffer to the encoder sector processor, and storing data encoded by the encoder sector processor into the buffer;
a subcode generator connected to the encoder buffer arbiter for generating sub-channel data;
a cross interleave reed-solomon code (CIRC) connected to the encoder buffer arbiter for generating main channel data;
a modulator connected to the subcode generator and the CIRC for converting the sub-channel data and the main channel data so as to generate a serial data stream;
a write controller connected to the modulator for converting the serial data stream into switch commands of write strategy; and
an absolute time in pre-groove decoder (ATIP decoder) connected to the write controller for providing absolute time information;

the encoding method comprising:
using the host interface to receive data from the computer;
using the encoder buffer arbiter to store data from the host interface into the buffer;
using the encoder buffer arbiter to transfer data in the buffer to the encoder sector processor;
using the encoder sector processor to encode data transmitted from the encoder buffer arbiter according to modes of the data;
using the encoder buffer arbiter to overwrite data stored in the buffer with data encoded by the encoder sector processor;
using the subcode generator to generate sub-channel data;
using the CIRC to interleave data encoded by the encoder sector processor and stored in the buffer so as to generate main channel data;
using the modulator to convert the sub-channel data and the main channel data so as to generate a serial data stream;
using the ATIP decoder to provide absolute time information; and
using the write controller to convert the serial data stream into switch commands of write strategy and outputting the switching commands with reference to the absolute time information.

[c5] 5.The encoding method of claim 4 wherein the encoder buffer arbiter comprises a trigger register for generating initial triggers and change mode triggers, the encoding method further comprising:
using the trigger register to output a change mode trigger to latch last data stored in the buffer so as to notify the encoder sector processor and the subcode generator that the last data and data following the last data need to be encoded with the next mode.

[c6] 6.The encoding method of claim 5 wherein the encoder buffer arbiter further comprises a buffer arbiter for accessing data stored in the buffer, and a data mode field register for storing a mode type of the next mode, the encoding method further comprising:
using the buffer arbiter to access data stored in the buffer; and
updating the data mode field register when receiving the change mode trigger

from the trigger register.

[c7] 7.The encoding method of claim 6 wherein the buffer arbiter is a DRAM arbiter.

[c8] 8.The encoding method of claim 5 wherein the encoder sector processor comprises a sector processor for encoding data transmitted from the encoder buffer arbiter, a first level encoder register for storing a data format of the current mode, and a second level encoder register for storing a data format of the next mode, the encoding method further comprising:
notifying the encoder sector processor that the last data and data following the last data need to be encoded with the next mode when receiving the latched data from the encoder buffer arbiter; and
loading the data format of the next mode from the second level encoder register into the first level encoder register.

[c9] 9.The encoding method of claim 4 wherein the buffer comprises a sector data area for storing data transmitted from the host interface and data encoded by the encoder sector processor, and a Q channel program page area for storing program codes for the subcode generator, the encoding method further comprising:
storing program codes of the current mode in a first storage space in the Q channel program page area; and
storing program codes of the next mode in a second storage space in the Q channel program page area.

[c10] 10.The encoding method of claim 9 wherein the subcode generator comprises a subcode source register for selecting a source of the sub-channel data, a sub-channel auto generator for generating sub-channel data, and a multiplexer for outputting sub-channel data, the encoding method further comprising:
using the subcode source register to select a source for receiving program codes from the Q channel program page area or receiving sub-channel data from the sector data area;
using the sub-channel auto generator to generate the sub-channel data according to the program codes if the Q-channel program page area is selected; and

using a multiplexer to output the sub-channel data received from the sub-channel auto generator if the Q-channel program page area is selected or the sub-channel data received from the sector data area if the sector data area is selected.

[c11] 11.The encoding method of claim 4 wherein the buffer is a dynamic random access memory (DRAM), and the encoder buffer arbiter is an encoder RAM arbiter.